BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently amended) A manufacturing method of a semiconductor integrated circuit device comprising a memory cell formed of a MISFET and a capacitor formed on a main surface of a semiconductor substrate, said method comprising the steps of:

(a) forming said MISFET on the main surface of said semiconductor substrate;

(b) forming an insulating film above said MISFET by a high density ~~the~~ plasma CVD method at a temperature of 450°C to 700°C;

(c) forming a trench by etching said insulating film;

(d) depositing a silicon film on said insulating film and in said trench, filling said trench by a photoresist, then etching back said silicon film on said insulating film and removing the silicon film ~~on~~from said insulating film to leave the silicon film only on an inner surface of said trench;

(e) forming a rugged surface silicon film on said silicon film on said inner surface of said trench to form a lower electrode of said capacitor on the inner wall of the trench; and

(f) forming a dielectric film on said rugged surface silicon film and on said insulating film and forming a plate electrode on said dielectric film.

2. (Previously presented) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein said rugged surface silicon film is formed by crystal grains which are grown from crystal nucleuses of silicon deposited on said silicon film.

Claim 3 (Cancelled)

4. (Previously presented) The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein said semiconductor integrated circuit device has a first area in which said memory cell is formed and a second area in which a logic circuit is formed, and said

manufacturing method of a semiconductor integrated circuit device comprises, before said step (b), the step of:

(e) forming, in said second area in which a logic circuit is formed, an n channel MISFET and a p channel MISFET constituting said logic circuit, each of said n channel MISFET and said p channel MISFET comprising a gate electrode containing n type impurity and a gate electrode containing p type impurity, respectively.

5. (Cancelled)

6. (Currently amended) A manufacturing method of a semiconductor integrated circuit device comprising a memory cell including a MISFET and a capacitor formed on a main surface of a semiconductor substrate, said method comprising the steps of:

(a) forming said MISFET on the main surface of said semiconductor substrate;

(b) depositing a first insulating film above said MISFET at a first temperature;

(c) depositing a second insulating film on said first insulating film at a second temperature between 450°C and

700°C that is higher than said first temperature by a high-density plasma CVD method;

(d) forming a trench by etching said first and second insulating films;

(e) depositing a silicon film on said second insulating film and in said trench, filling said trench by a photoresist, then etching back said silicon film on said second insulating film and removing the silicon film on said second insulating film to leave the silicon film only on an inner surface of said trench;

(f) forming a rugged surface silicon film on said silicon film on said inner surface of said trench to form a lower electrode of said capacitor on the inner wall of the trench; and

(g) forming a dielectric film on said rugged surface silicon film and on said second insulating film and forming a plate electrode on said dielectric film.

Claims 7-9 (Cancelled)

10. (Previously presented) The manufacturing method of a semiconductor integrated circuit device according to claim 6,

wherein said semiconductor integrated circuit device has a first area in which said memory cell is formed and a second area in which a logic circuit is formed, and said manufacturing method of a semiconductor integrated circuit device comprises, before said step (b), the step of:

(h) forming, in said second area in which a logic circuit is formed, an n channel MISFET and a p channel MISFET constituting said logic circuit, each of said n channel MISFET and said p channel MISFET comprising a gate electrode containing n type impurity and a gate electrode containing p type impurity, respectively.

11. (Currently amended) A manufacturing method of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a MISFET on a main surface of a semiconductor substrate;

(b) ~~forming an insulating film containing impurity above said MISFET by a high density plasma CVD method at a temperature of 450°C to 700°C;~~ forming a plug connected with said MISFET through a first insulating film which has a substantially planarized surface;

(c) ~~forming a trench by etching said insulating film;~~forming a second insulating film containing impurity over said first insulating film by a high-density plasma CVD method at a temperature of 450°C to 700°C;

(d) forming a trench by etching said second insulating film;

~~(d)~~ (e) depositing a silicon film on said second insulating film and in said trench, filling said trench by a photoresist, then etching back said silicon film on said second insulating film, and removing the silicon film on said second insulating film to leave the silicon film only on an inner surface of said trench;

~~(e)~~ (f) forming a rugged surface silicon film on said silicon film ~~on said inner surface of said trench~~ to form a lower electrode of a capacitor on the inner wall of the trench; and

~~(f)~~ (g) forming a dielectric film on said rugged surface silicon film and on said second insulating film and forming a plate electrode on said dielectric film.

12. (Previously presented) The manufacturing method of a semiconductor integrated circuit device according to claim 11, wherein said impurity is phosphorus.

13. (Cancelled)

14. (Currently amended) A manufacturing method of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a MISFET on a main surface of a semiconductor substrate;

(b) depositing a first insulating film above said MISFET at a first temperature;

(c) planarizing a surface of said first insulating film;

(d) forming a second insulating film containing impurity on said first insulating film at a second temperature higher than said first temperature by a high-density plasma CVD method;

(e) forming a trench by etching said first and second insulating films;

(f) depositing a silicon film on said second insulating film and in said trench, filling said trench by a photoresist, then etching back said silicon film on said second insulating film, and removing the silicon film on said second insulating film to leave the silicon film only on an inner surface of said trench;

(g) forming a rugged surface silicon film on said silicon film on said inner surface of said trench to form a lower electrode of a capacitor on the inner wall of the trench; and

(h) forming a dielectric film on said rugged surface silicon film and on said second insulating film and forming a plate electrode on said dielectric film.

15. (Previously presented) The manufacturing method of a semiconductor integrated circuit device according to claim 14, wherein said impurity is phosphorous.

16. (Previously presented) The manufacturing method of a semiconductor integrated circuit device according to claim 14, wherein said first and second insulating films are formed by the CVD method using high-density plasma.

17. (Withdrawn) A semiconductor integrated circuit device, comprising:

(a) a MISFET formed on a main surface of a semiconductor substrate; and

(b) a capacitor connected in series to said MISFET, wherein said capacitor comprises:

(b1) a lower electrode made of a silicon film, which is formed at a concave portion in a lamination layer of a first insulating film formed above said MISFET and a second insulating film formed on said first insulating film and having smaller impurity content than said first insulating film;

(b2) a capacitor insulating film formed on said lower electrode; and

(b3) an upper electrode formed of a conductive film.

18. (Withdrawn) A semiconductor integrated circuit device, comprising:

(a) a MISFET formed on a main surface of a semiconductor substrate; and

(b) a capacitor connected in series to said MISFET, wherein said capacitor comprises:

(b1) a lower electrode made of a silicon film, which is formed at a concave portion in a lamination layer of a first insulating film formed above said MISFET and a second insulating film which is thinner than said first insulating film and formed on said first insulating film;

(b2) a capacitor insulating film formed on said lower electrode; and

(b3) an upper electrode formed of a conductive film formed on said capacitor insulating film.

19. (Withdrawn) The semiconductor integrated circuit device, according to claim 18,

wherein said second insulating film has a smaller impurity content than said first insulating film.